

CTAデュアルミラー光学系用 焦点面検出器の試作器開発

Hiro Tajima, Akira Okumura, Naoya Hidaka, Takanori Kawashima

Solar-Terrestrial Environment Laboratory, Nagoya University

Stefan Funk, Leonid Sapozhnikov, Luigi Tibaldo

SLAC National Accelerator Laboratory

Kavli Institute for Particle Astrophysics and Cosmology

Justin Vandenbroucke

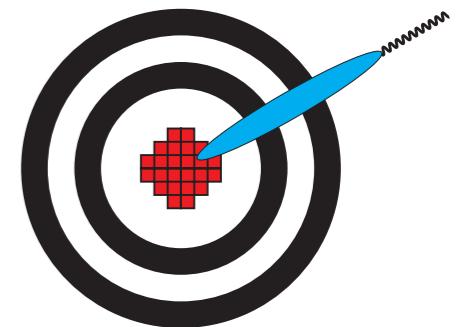
University of Wisconsin, Madison

Richard White, Jim Hinton

Department of Physics and Astronomy, University of Leicester

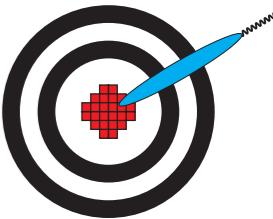


WISCONSIN
UNIVERSITY OF WISCONSIN-MADISON

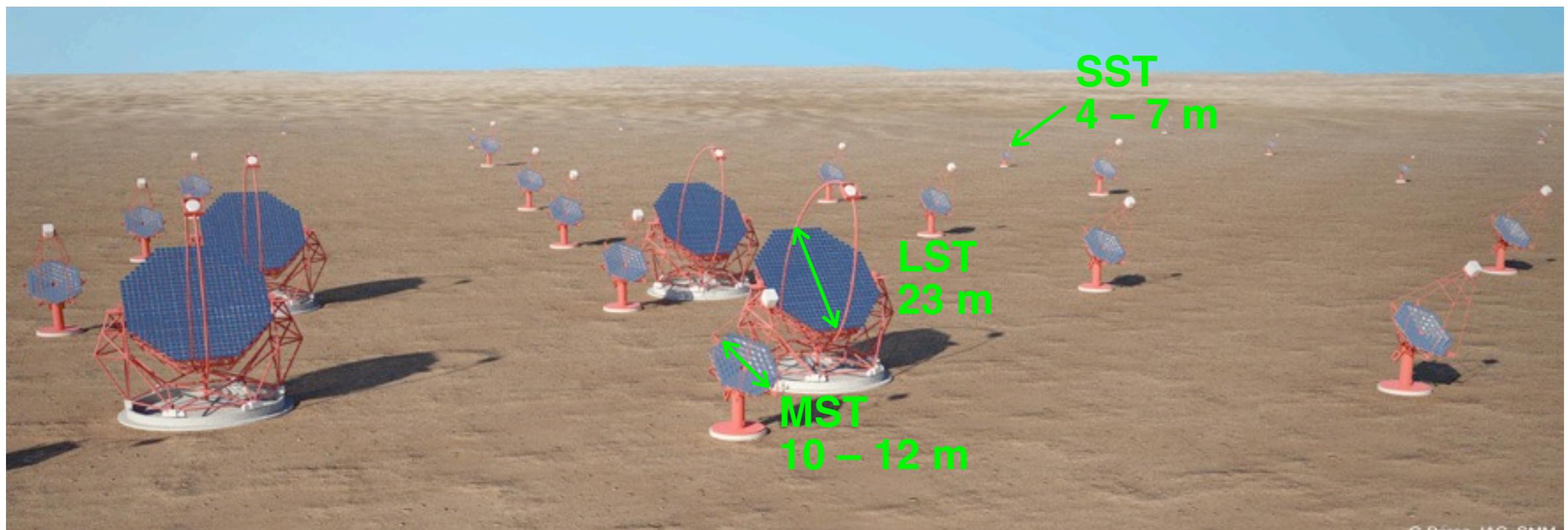


September 20, 2013
JPS meeting
高知

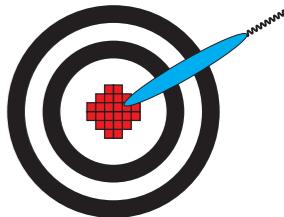
Cherenkov Telescope Array



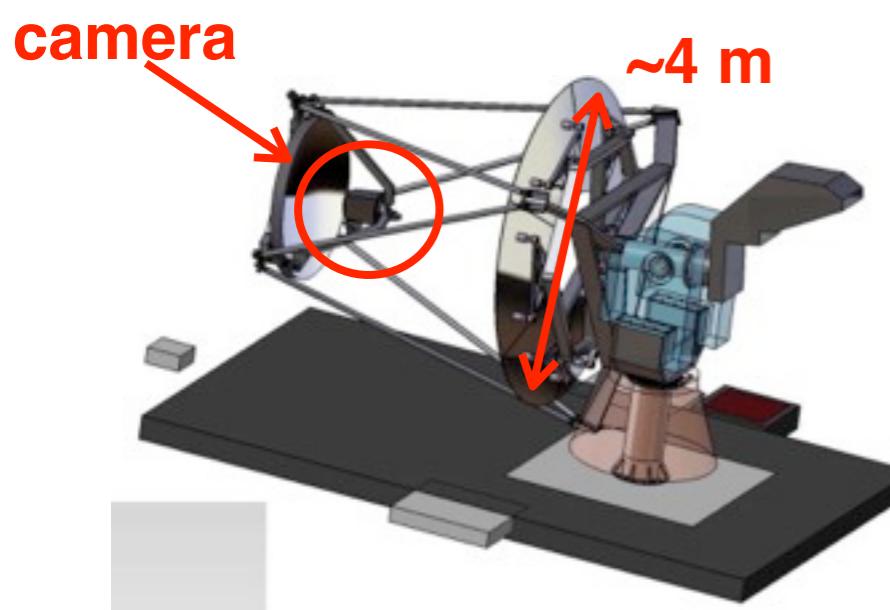
- ❖ Observations of gamma rays in 20 GeV – 100 TeV band
 - ✿ Cherenkov light from electromagnetic shower produced by interaction of gamma rays with atmosphere
- ❖ Large collection area by placing many telescopes
 - ✿ x10 better sensitivity
- ❖ Wide energy band coverage by three different size of telescopes
 - ✿ Large-size telescope (LST): $\Phi = 23 \text{ m}$, 20 GeV – 1 TeV, 4 telescopes
 - ✿ Medium-size telescope (MST): $\Phi = 10 - 12 \text{ m}$, 0.1 – 10 TeV, ~20 telescopes
 - ✿ Small-size telescope (SST): $\Phi = 4 - 7 \text{ m}$, 1 – 100 TeV, 30 – 70 telescopes



SC-MST/SST Design Concept

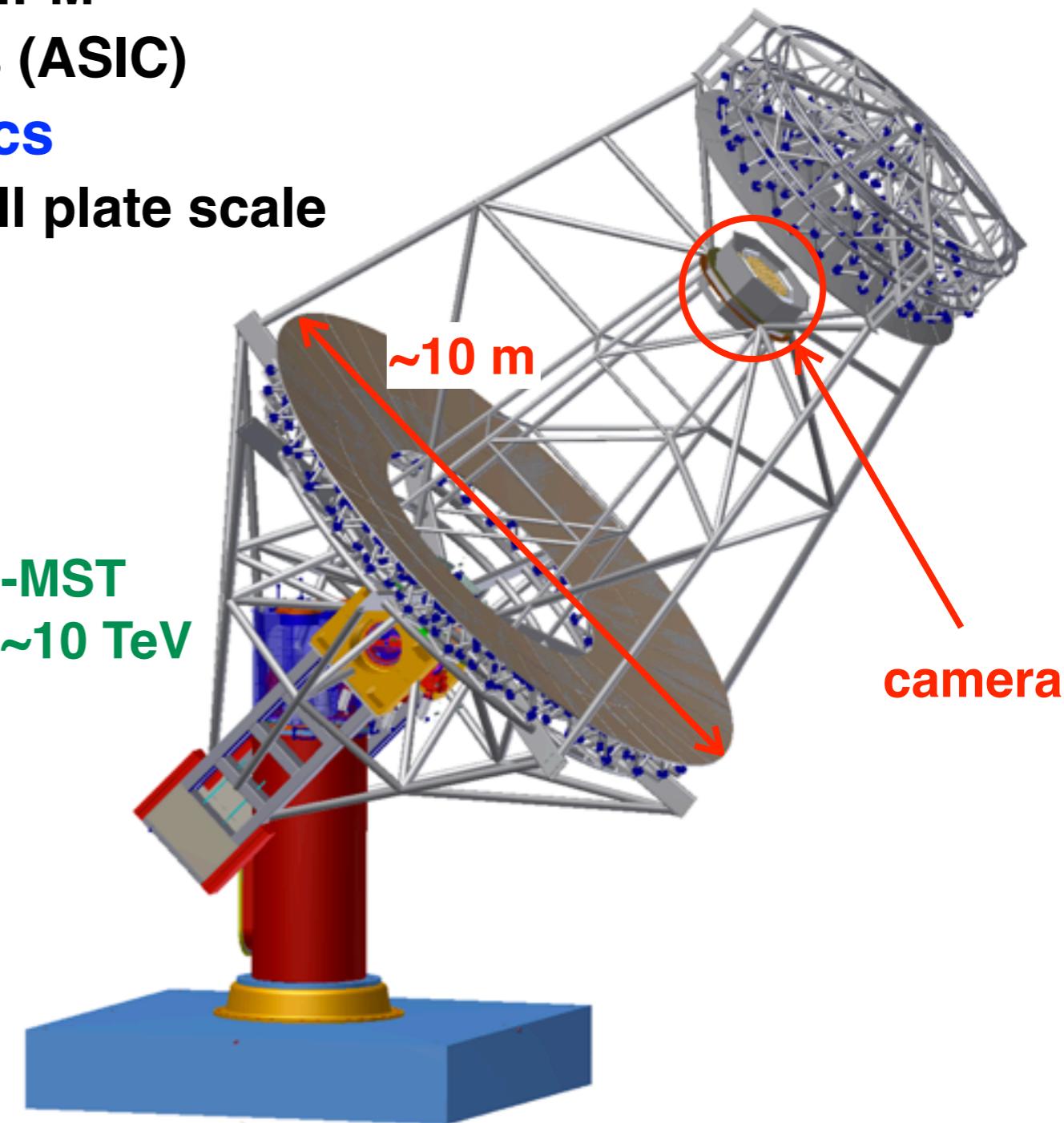


- ❖ Dual mirror design with small pixel photon sensor
 - ✿ Small pixel (~6 mm) photon sensor to reduce camera cost
 - ◆ Multi-anode photomultiplier or SiPM
 - ◆ High density readout electronics (ASIC)
 - ✿ Schwarzschild-Couder (SC) optics
 - ◆ Short focal length to realize small plate scale
 - Technically challenging
 - ◆ Large field of view
 - Longer telescope spacing (larger collection area)

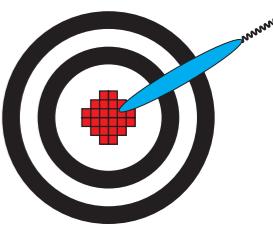


SC-SST
1~100 TeV

SC-MST
0.1~10 TeV



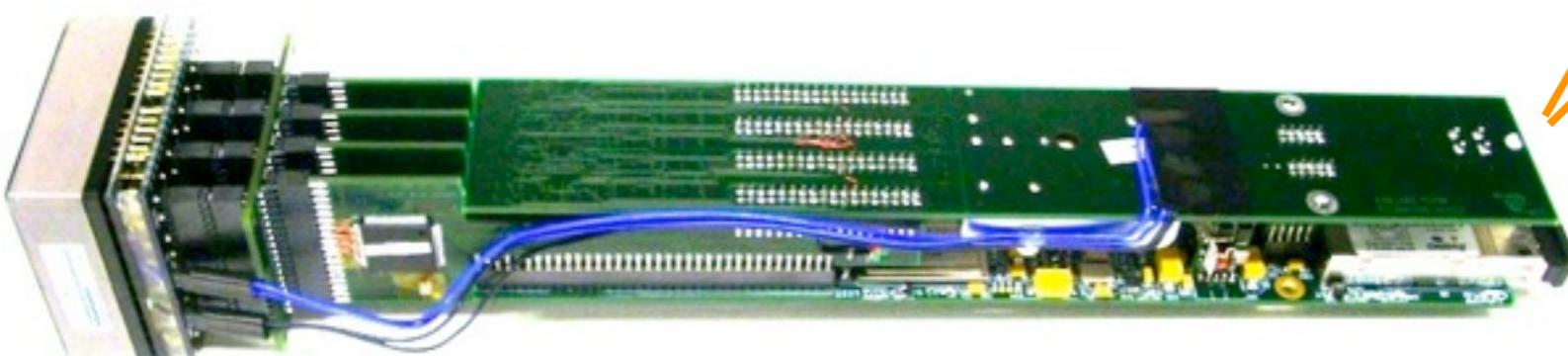
SC-SST Camera Design



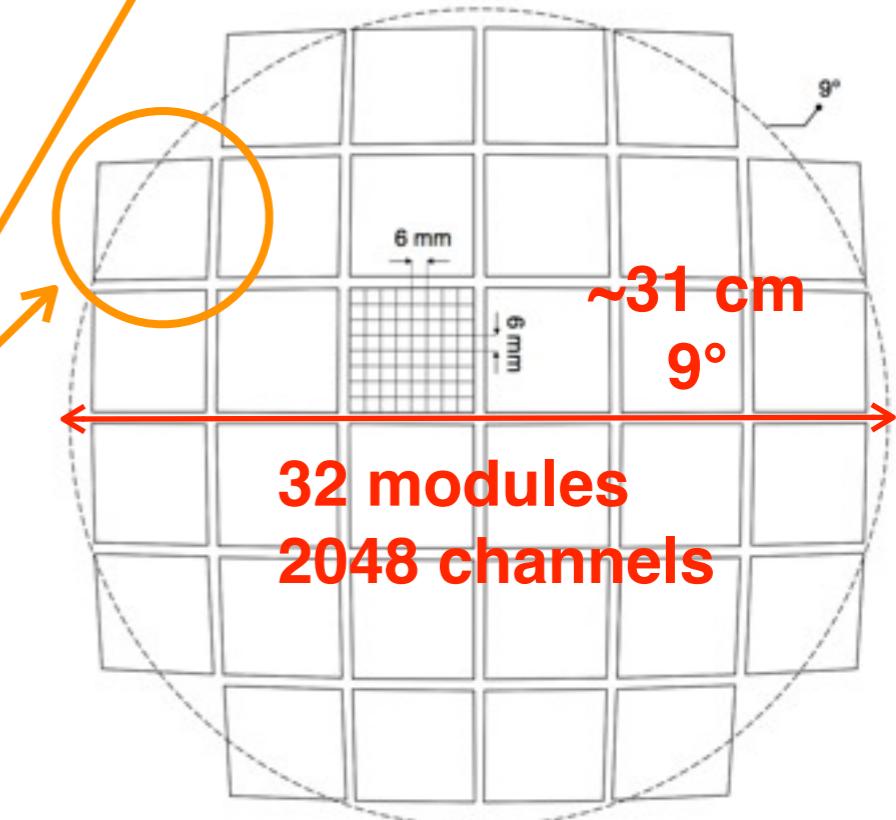
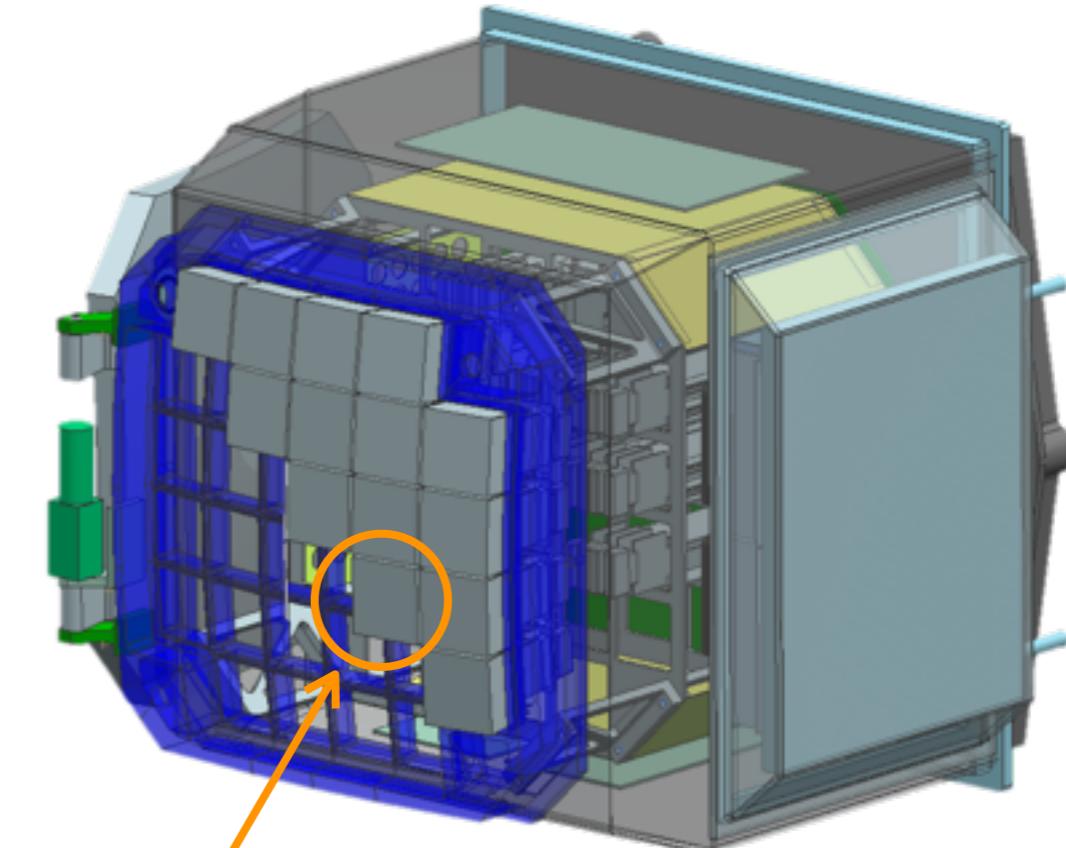
❖ SC-SST camera parameters

	32 mod
FOV for 0.18°/pixel (36 mm/°)	8.6°
FOV for 0.28°/pixel (23 mm/°)	13.4°
Angular pixel size for FOV=10°	0.21°
# of pixels per camera	2,048
Power consumption per camera (FE)	350 W
Weight per camera (FE+SiPM)	11 kg
Total cost (FE+SiPM) for 50 CAMs*	\$7.2M

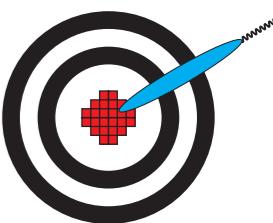
*Assuming \$20/ch, which does not explicitly include labor for mechanical module assembly and calibrations



Front-End (FE) electronics module

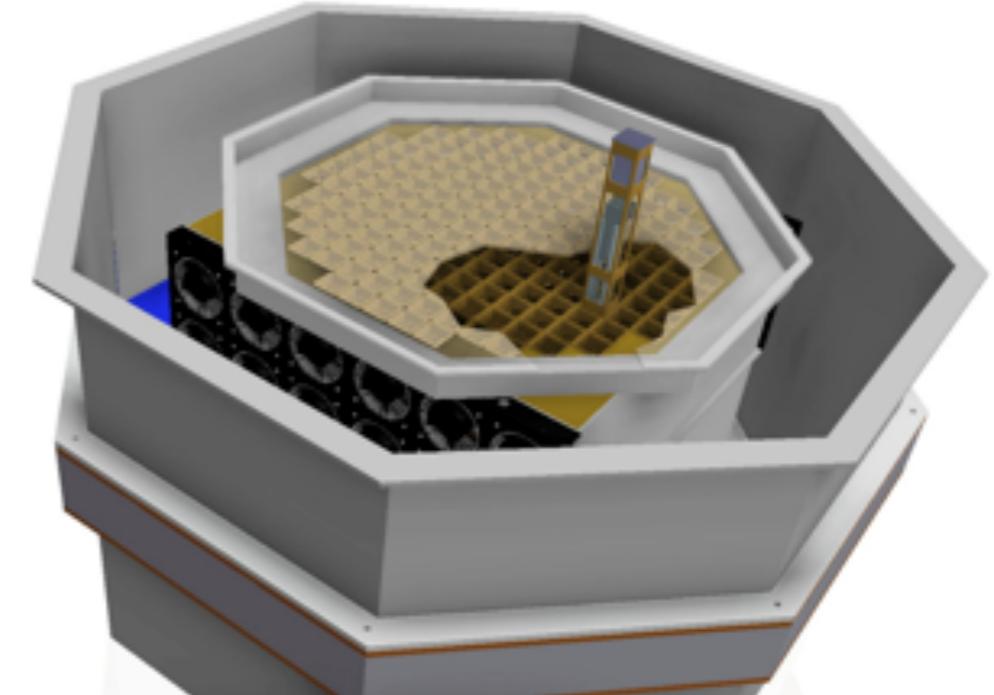


SC-MST Camera Design

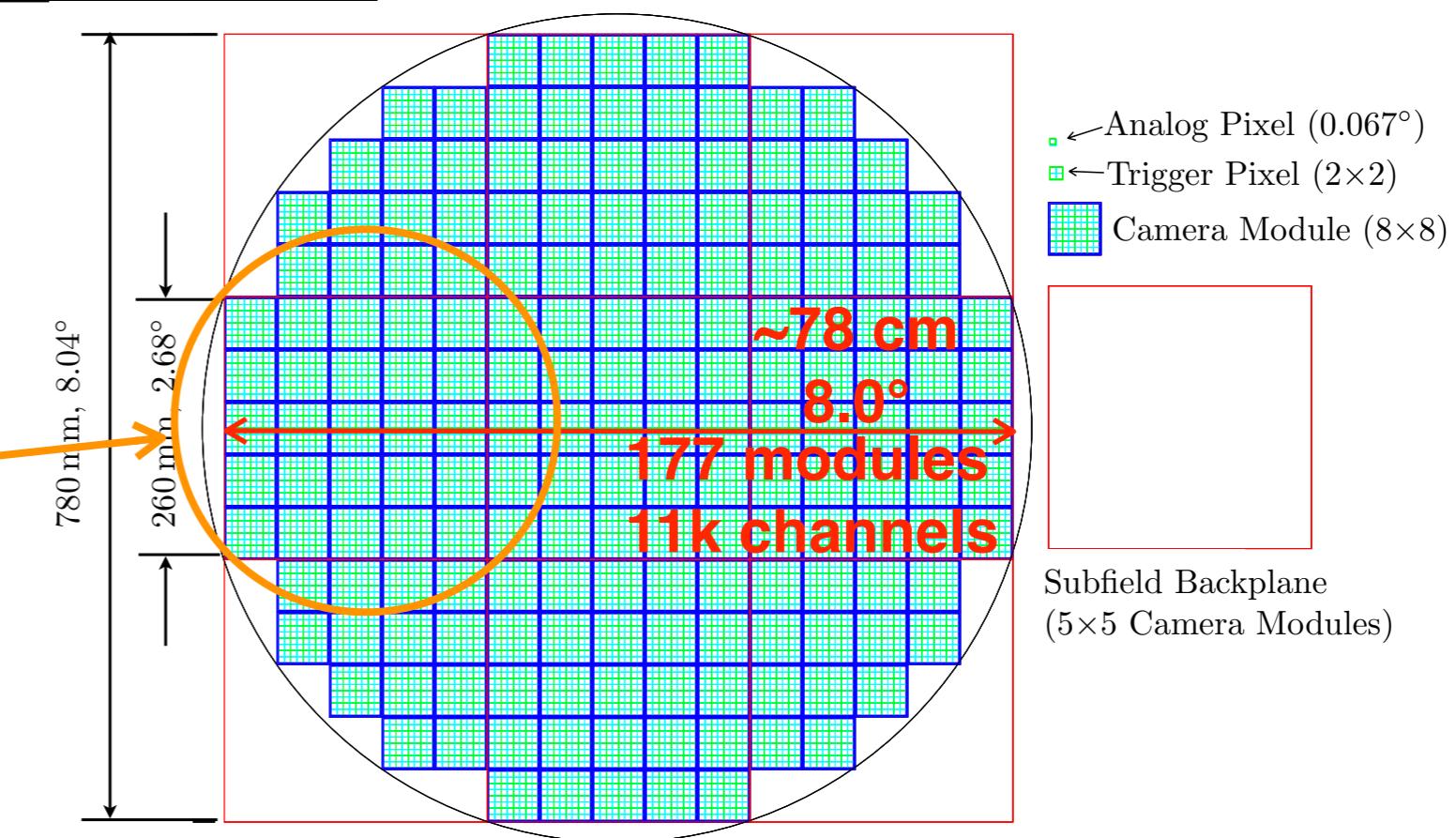
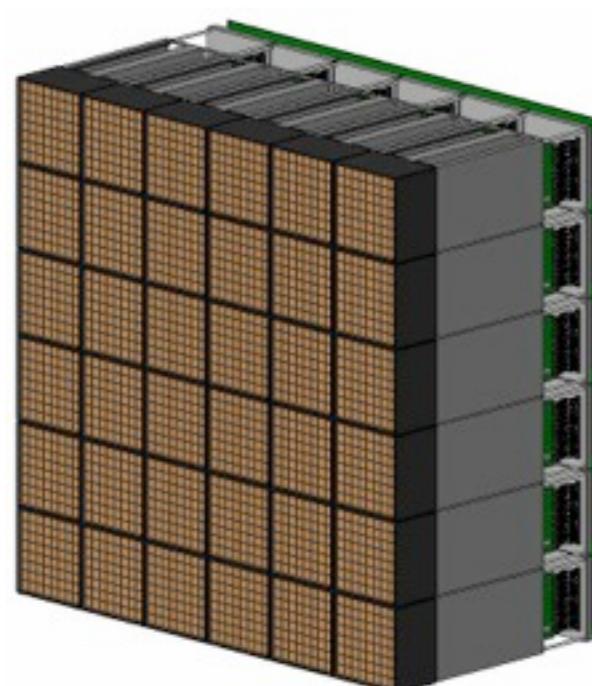


❖ SC-MST camera parameters

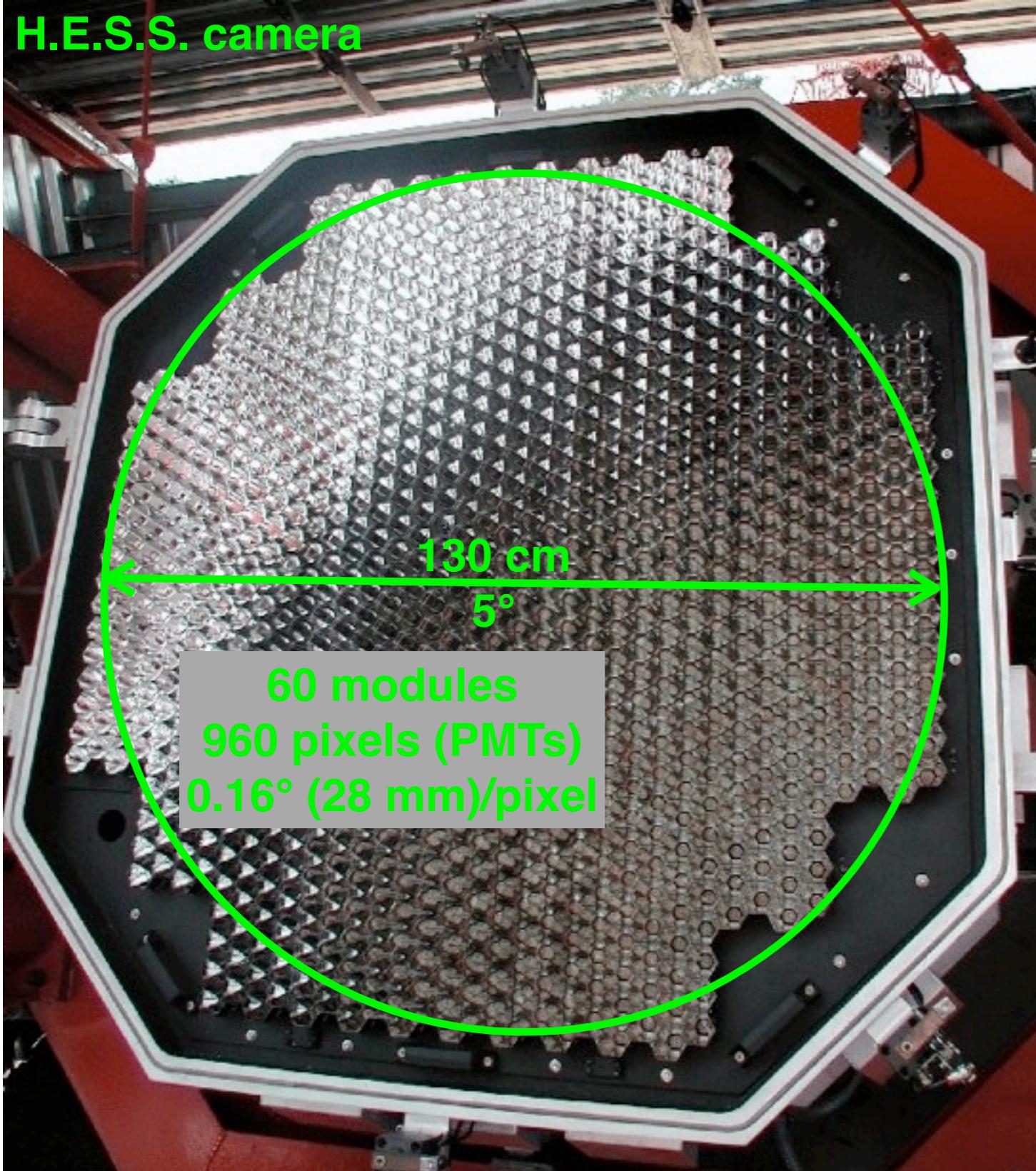
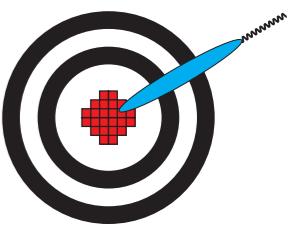
FOV	8.0°
Angular pixel size	0.067°
# of pixels per camera	11,328
Power consumption per camera (FE)	2000 W
Weight per camera (FE+SiPM)	61 kg
Total cost (FE+SiPM) for 50 CAMs*	\$24M



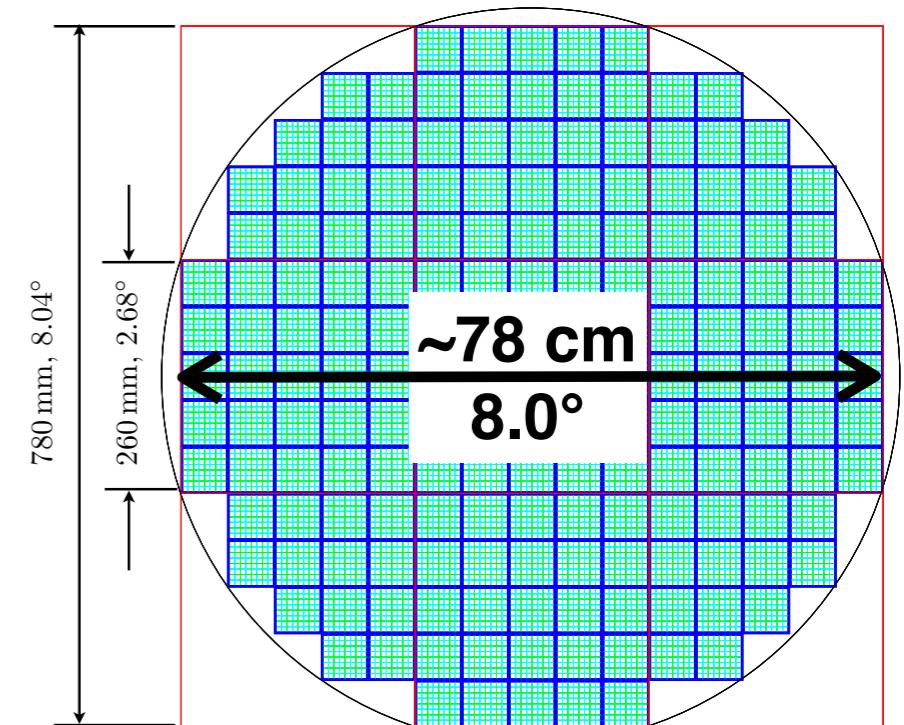
*Assuming \$20/ch, which does not explicitly include labor for mechanical module assembly and calibrations



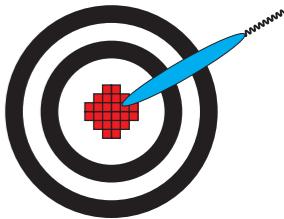
Comparison with Existing Cherenkov Camera



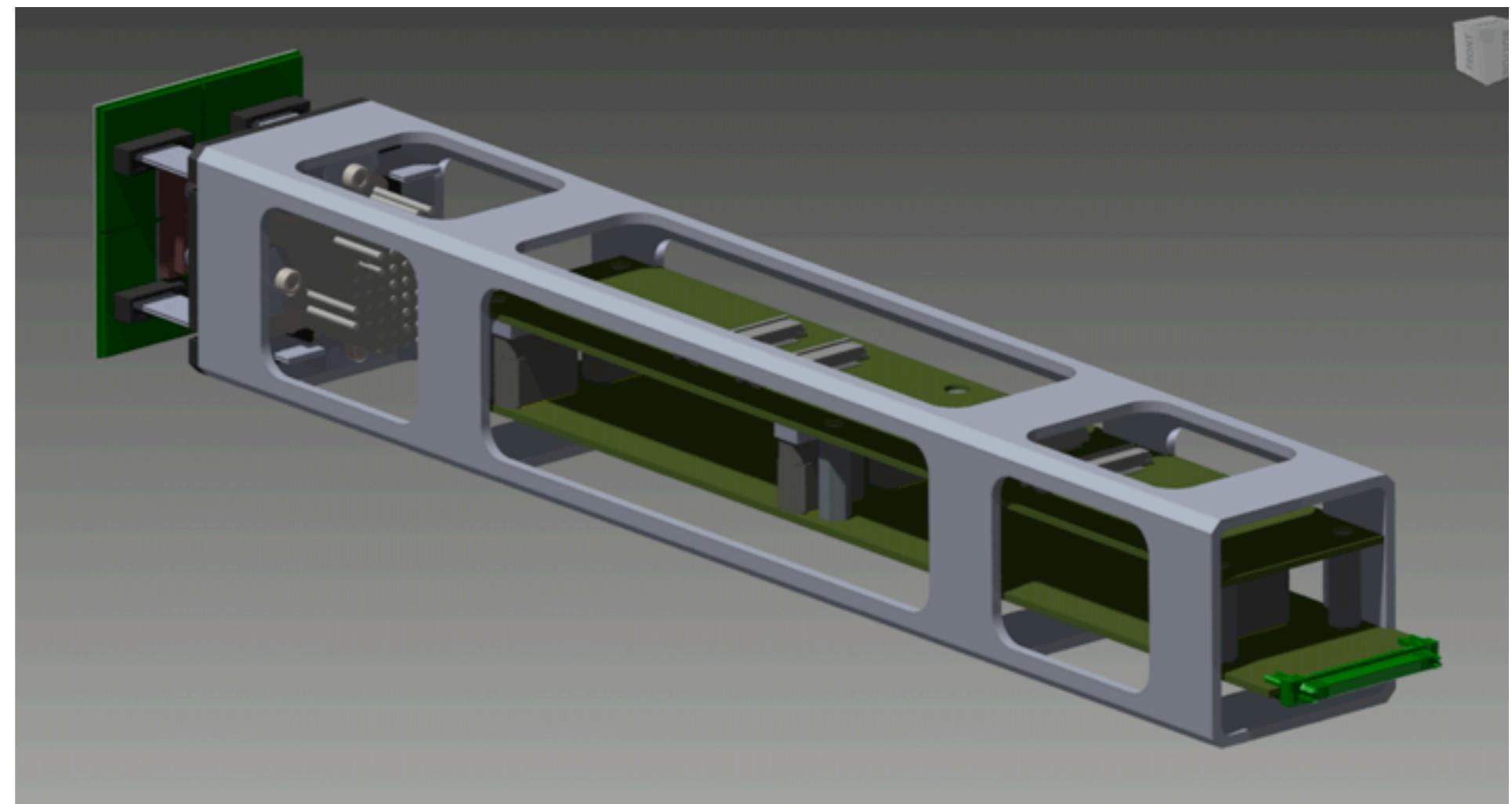
SC-MST camera



177 modules
11k pixels
0.064° (6.2 mm)/pixel

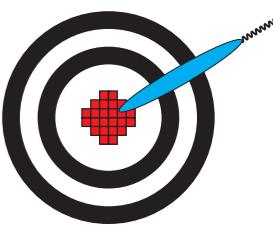


- ❖ **Board configuration**
 - ✿ Photosensor I/F board: preamp, high voltage (HV), Peltier control
 - ✿ Signal processing board: TARGET ASIC, FPGA, back-end I/F, power supply
- ❖ **Minimize # of components for cost reduction and reliability**
 - ✿ Integration of necessary functionalities into an ASIC

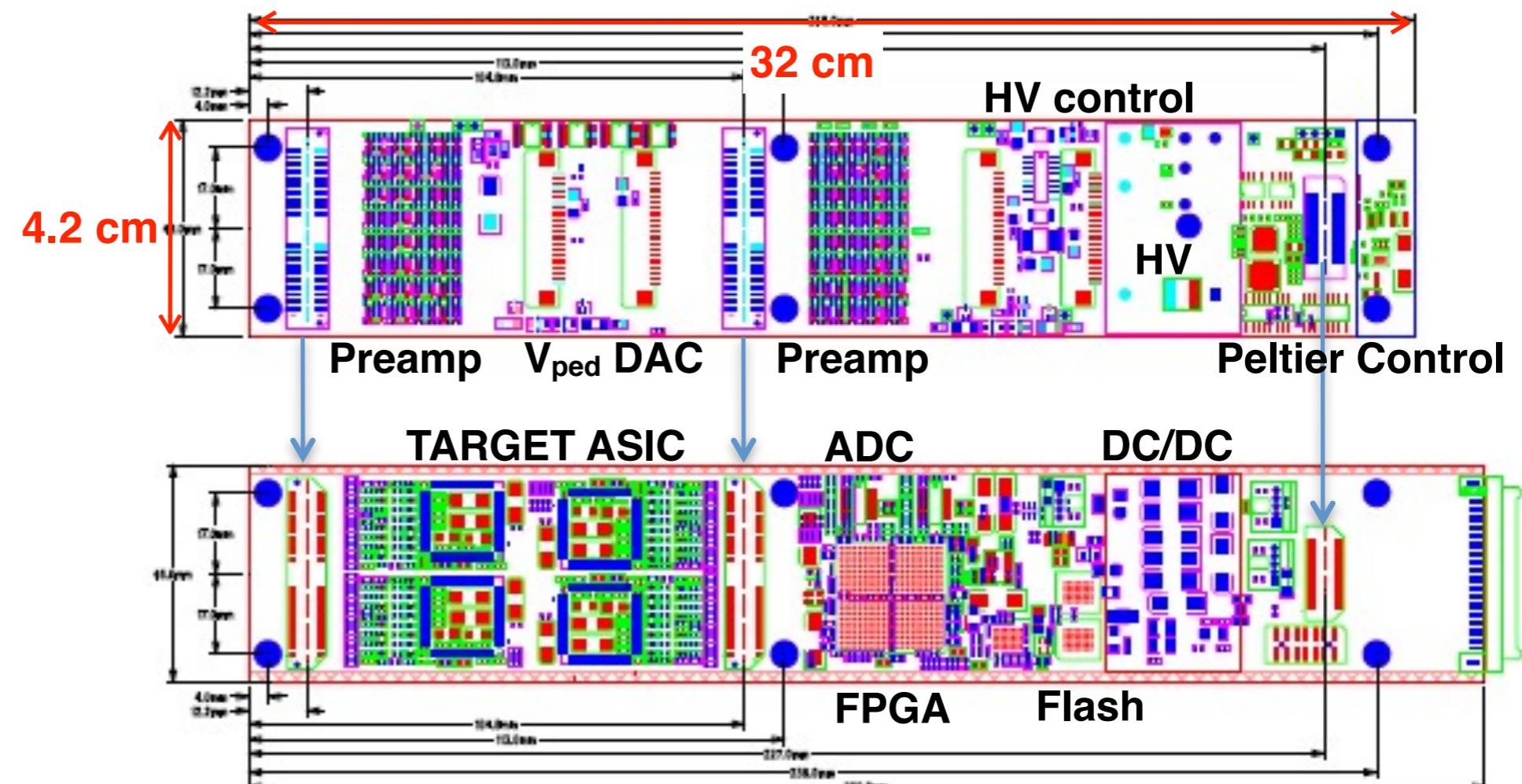


designed by G. Varner
(Hawaii)

SC Camera Front-End Electronics



- ❖ Board configuration
 - ✿ Photosensor I/F board: preamp, high voltage (HV), Peltier control
 - ✿ Signal processing board: TARGET ASIC, FPGA, back-end I/F, power supply
- ❖ Minimize # of components for cost reduction and reliability
 - ✿ Integration of necessary functionalities into an ASIC

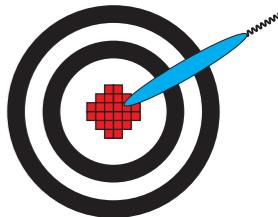


designed by G. Varner
(Hawaii)

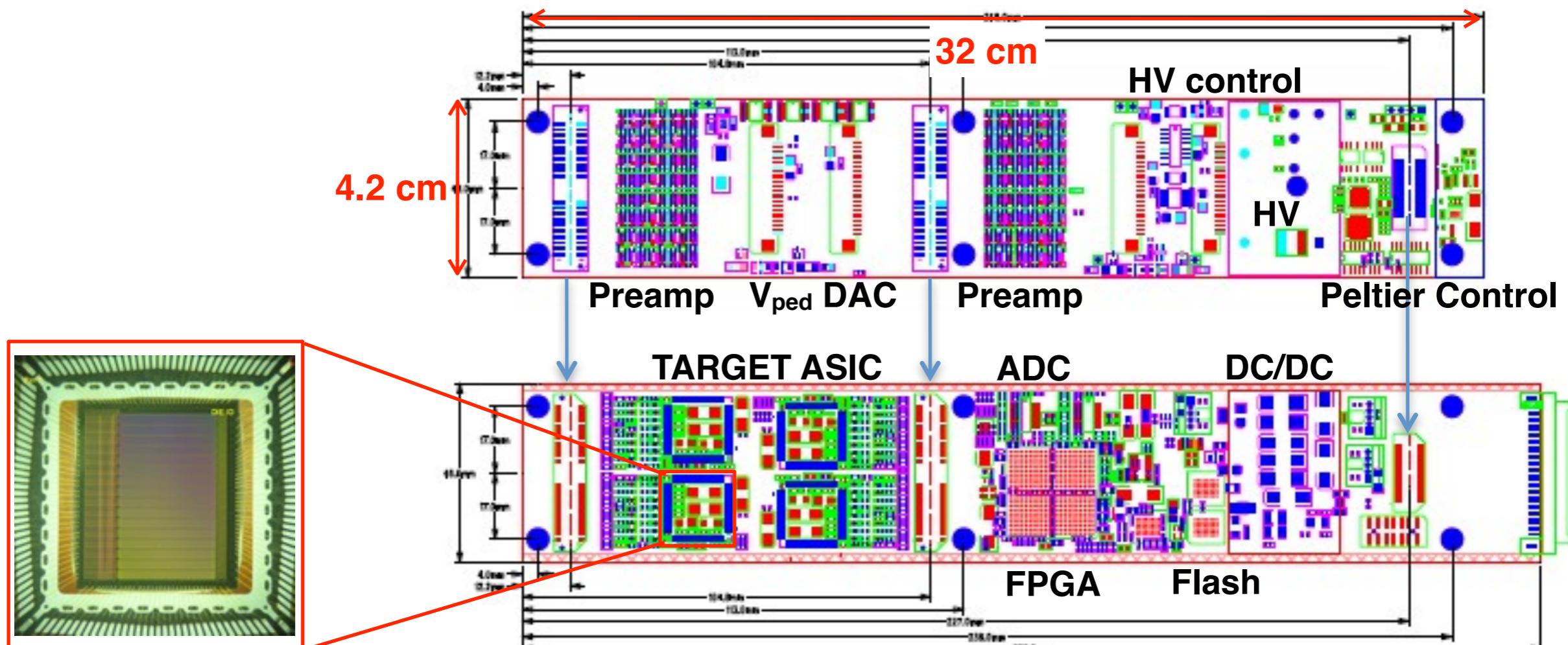
CTAデュアルミラー光学系用焦点面検出器の試作器開発

JPS meeting, SEP 20, 2013, 高知

SC Camera Front-End Electronics

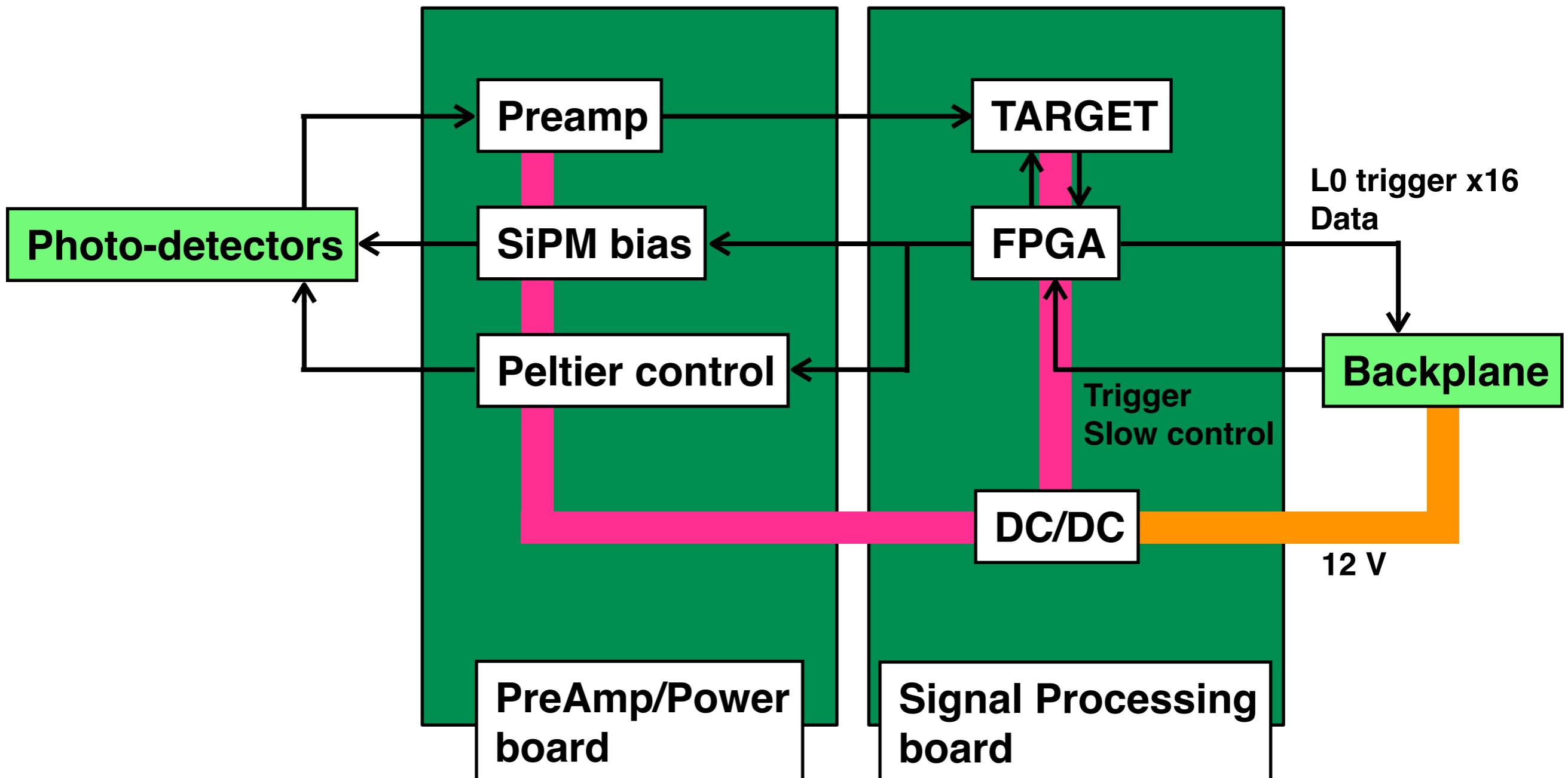
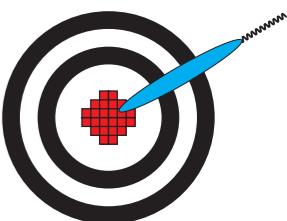


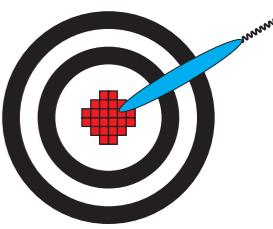
- ❖ Board configuration
 - ✿ Photosensor I/F board: preamp, high voltage (HV), Peltier control
 - ✿ Signal processing board: TARGET ASIC, FPGA, back-end I/F, power supply
- ❖ Minimize # of components for cost reduction and reliability
 - ✿ Integration of necessary functionalities into an ASIC



designed by G. Varner
(Hawaii)

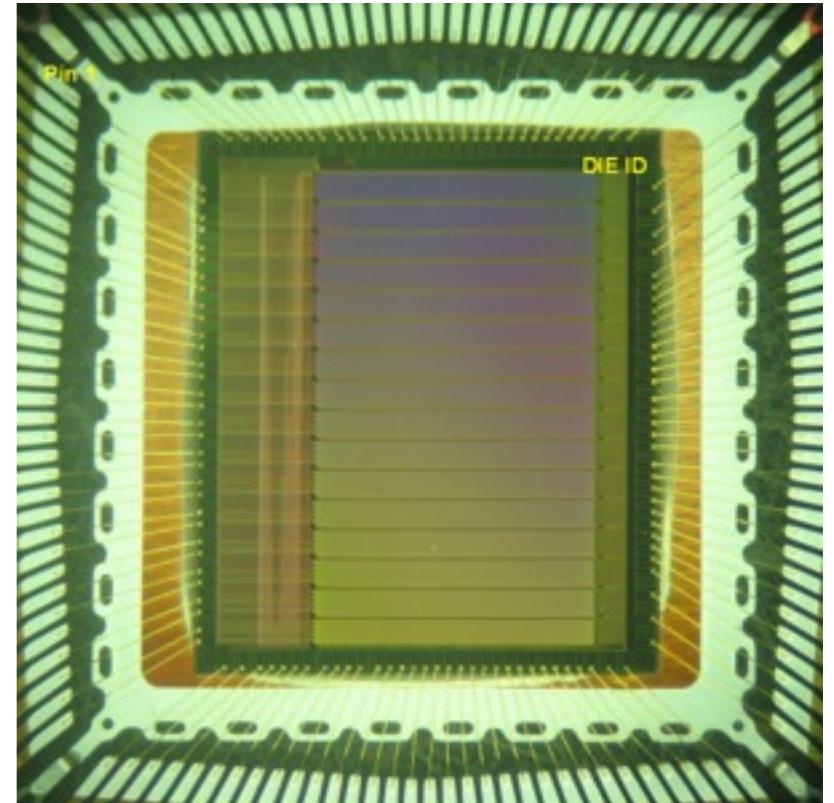
FEE Function Diagram





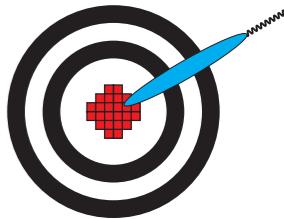
❖ Requirements

- ❖ **Waveform sampling at $\sim 1 \text{ GSa/s}$**
- ❖ **Signal bandwidth $> 380 \text{ MHz}$**
- ❖ **Cross-talk $< 1\%$**
- ❖ **Look-back time: $> 12 \mu\text{s}$**
- ❖ **Dynamic range: $> 9 \text{ bits}$**
- ❖ **Readout (dead) time: $< 30 \mu\text{s}$**
- ❖ **Trigger timing: $< 4 \text{ ns}$**
- ❖ **Trigger segment: $0.1^\circ \times 0.1^\circ \sim 0.2^\circ \times 0.2^\circ$**



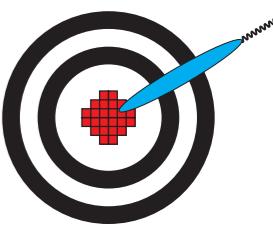
❖ TARGET ASIC

- ❖ **Switched capacitor array for high speed waveform sampling**
- ❖ **Integrated digitization circuits and trigger circuits**
 - ◆ Reduction of components and cost, increase reliability
- ❖ **Internal bias generator**
 - ◆ All digital interface
- ❖ **Low power consumption: $\sim 70 \text{ mW/channel}$ including FPGA**

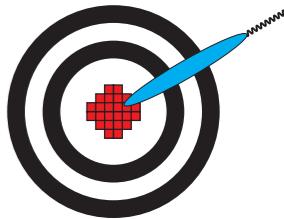


- ❖ TARGET-1
 - ✿ 2008/May delivery
 - ✿ BW is limited to ~150 MHz, 8k cells, no analog sum trigger
- ❖ TARGET-2/TARGET-4
 - ✿ 2011/Aug (TARGET-2), 2012/Feb (TARGET-4)
 - ✿ Improved BW and cross talk, 16k cells, more (faster) digitization circuits, 4-ch analog sum trigger
 - ✿ Problem with serial register loading, DAC voltage routing
- ❖ TARGET-5
 - ✿ 2012/Aug delivery
 - ✿ BW is confirmed up to 400 MHz, cross talk < 1%
 - ✿ Minimum trigger threshold is too high (~25 mV, ~6 p.e.)
- ❖ TARGET-7
 - ✿ 2013/Sep submission, Dec delivery (expected)
 - ✿ Wider dynamic range, better linearity and better temperature stability
 - ✿ Lower trigger threshold (<10 mV, 2.5 p.e.)

TARGET-7 Specifications



	TARGET-5	TARGET-7
# of channels	16	16
# of cells/channel	16,384	16,384
Sampling frequency	0.4 – 1.2 GHz	0.5, 1.0 GHz
Bandwidth	> 380 MHz	> 380 MHz
Crosstalk (@ -3dB)	< 1%	< 1%
Dynamic range	0.6–1.0 mV/1.5 V	0.6–1.0 mV/2 V
Wilkinson ADC clock speed	~700 MHz	~500 MHz (external, both edges)
Digitization time	5.9 μ s (12 bit)	8.2 μ s (12 bit)
# of cells/digitization	32 cells x 16 ch	32 cells x 16 ch
Data transfer speed	~90 Mbps x 16 ch	~90 Mbps x 16 ch
Dead time (48 cells/ch)	10 bit 2.9 + 8 μ s 12 bit 11.7 + 8 μ s	4.1 + 8 μ s 16.4 + 8 μ s
# of trigger output	4 (4 ch analog sum) + 1 (16 ch analog sum)	4 (4 ch analog sum, no gain adjustment)
Trigger threshold at input	25 mV minimum	10 – 80 mV (2.5 – 20 p.e. for MST) 0.2 mV step (nominal, 0.05 p.e. for MST)
Trigger threshold noise	< 4 mV	< 1.6 mV (rms)
Trigger gain adjustment	20%	None



❖ SC-MST prototype

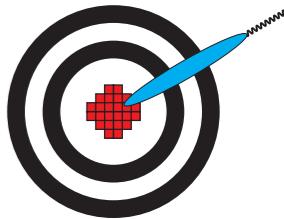
- ✿ **Partially populated mirrors and SiPM camera modules**
 - ◆ Comprehensive study of the structure, mirrors, motorization and control system

❖ SC-SST prototype

- ✿ **Mini-array: 5 complete telescopes and cameras**
 - ◆ 1 MAPM camera + 4 SiPM cameras
- ✿ **Test array performance, conduct scientific observations**

	2013		2014				2015			
	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	
SC-SST	32x MAPM modules	MAPM camera assembly		lab test	field test			Mini-array		
		32x SiPM modules	SiPM camera assembly		lab test	field test				
SC-MST		25x SiPM modules	SiPM camera assembly	lab test	field test					

Summary and Plans



- ❖ **Waveform sampling capability of TARGET-5 is satisfactory**
 - ✿ Trigger performance will be fixed by TARGET-7 with better dynamic range and linearity
- ❖ **Characterization and improvement of SiPM ongoing**

22pSD7: 日高直哉

「CTA計画 半導体光検出器MPPCを用いたチェレンコフカメラの開発」

- ❖ **Plans**
 - ✿ TARGET-7 will be submitted for fabrication in 2013/Sep
 - ✿ Prototype production started
 - ◆ SC-SST mini-array
 - ◆ SC-MST partial telescope